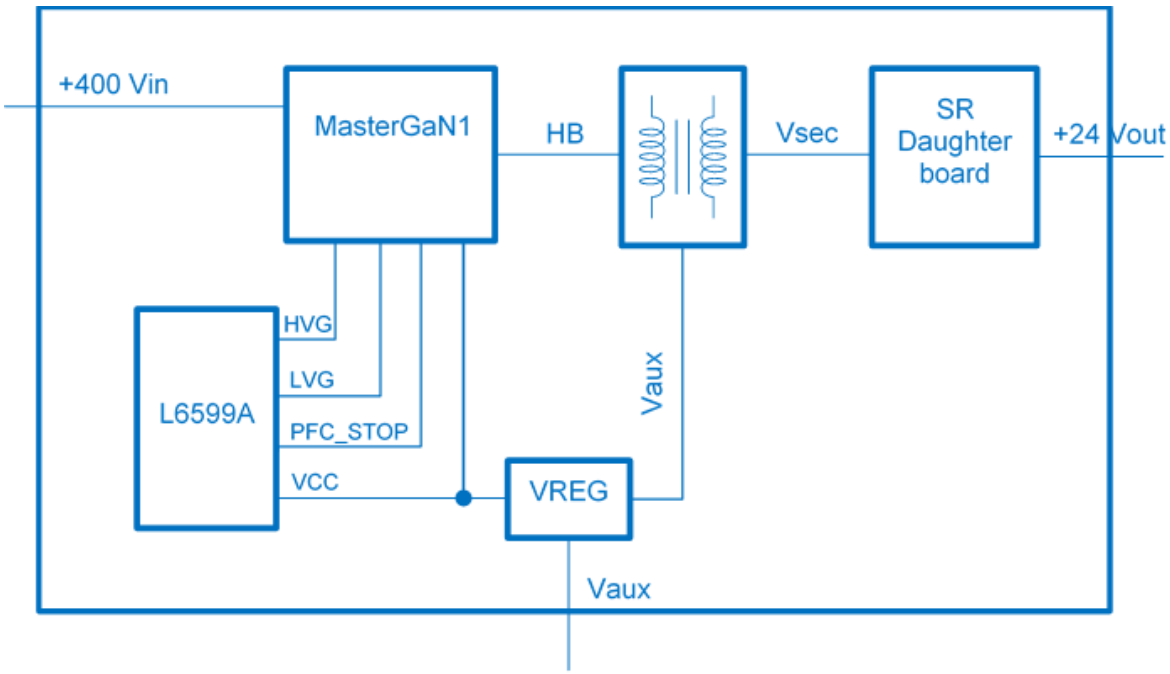
DC/DC resonant converter for industrial applications using MasterGaN1

Introduction

This evaluation board is a resonant LLC converter dedicated to any kind of industrial application where minimum size and high efficiency are required (industrial DC/DC applications, adapters, consumer SMPS), based on the MasterGaN1. This device, embedding a couple of GaN power transistors and a driver in the same package, allows to directly interface any kind of SMPS controller. Thanks to the GaN technology and to the embedded driver, the converter can be designed with an operating frequency higher than using conventional MOSFET's. Actually the board has no heatsink on the primary side and has very reduced dimensions. The high efficiency and small size make the board very suitable when available space is limited; the power density is 20 W/inch^3. Output power can be up to 250 W at 24 Vdc, nominal input voltage is 400 V as delivered by conventional front-end PFCs. The board comes with overcurrent, short-circuit and voltage loop fail protection. The integrated input voltage monitoring allows the LLC converter startup with correct sequencing, preventing operation with too low input voltage.

Figure 1. EVLMG1-250WLLC evaluation board

Figure 2. **EVLMG1-250WLLC: functional block diagram**



1 EVLMG1-250WLLC schematic

Figure 3. **EVLMG1-250WLLC motherboard schematic**

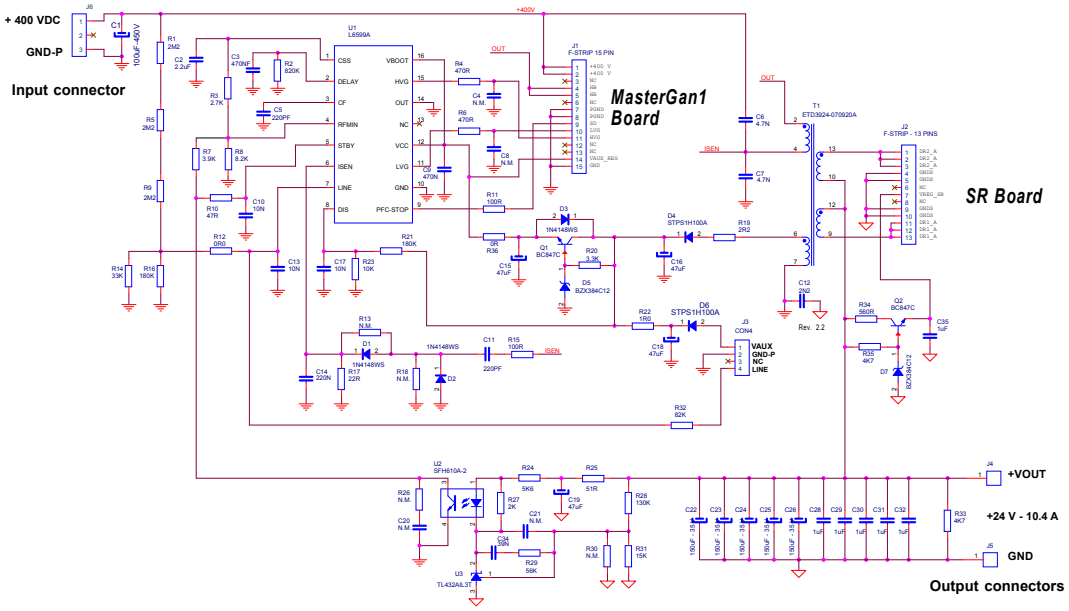


Figure 4. **EVLMG1-250WLLC MasterGaN1 module schematic**

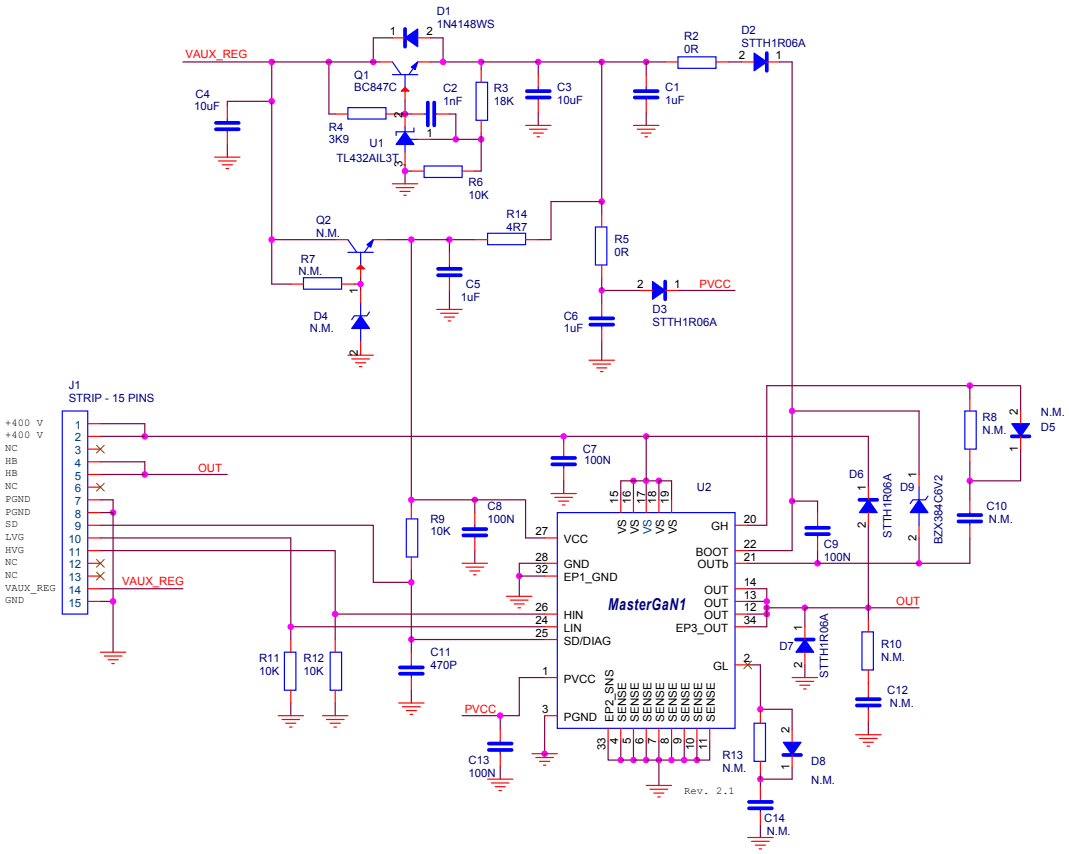
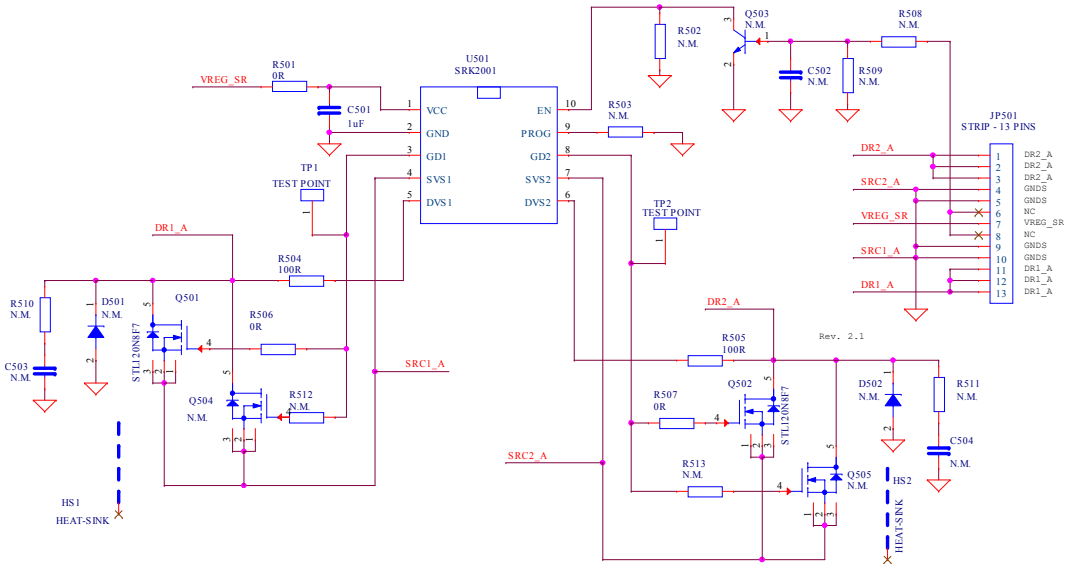


Figure 5. **EVLMG1-250WLLC SRK module schematic**



2 EVLMG1-250WLLC PCB layout

Figure 6. **EVLMG1-250WLLC motherboard PCB tracks – top side**

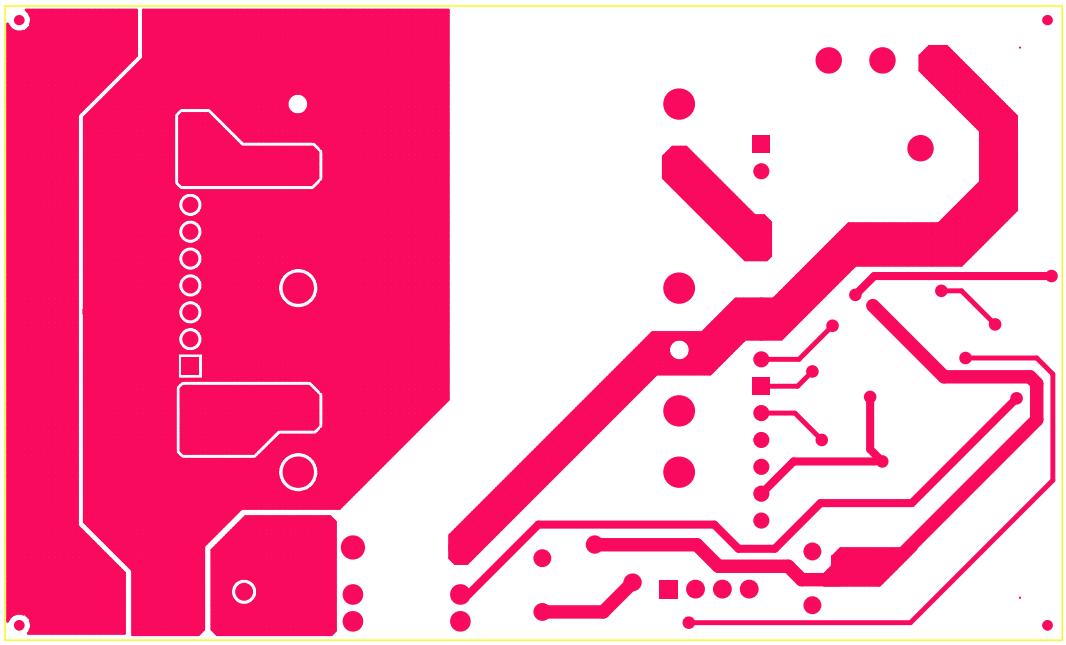


Figure 7. **EVLMG1-250WLLC motherboard PCB tracks – bottom side**

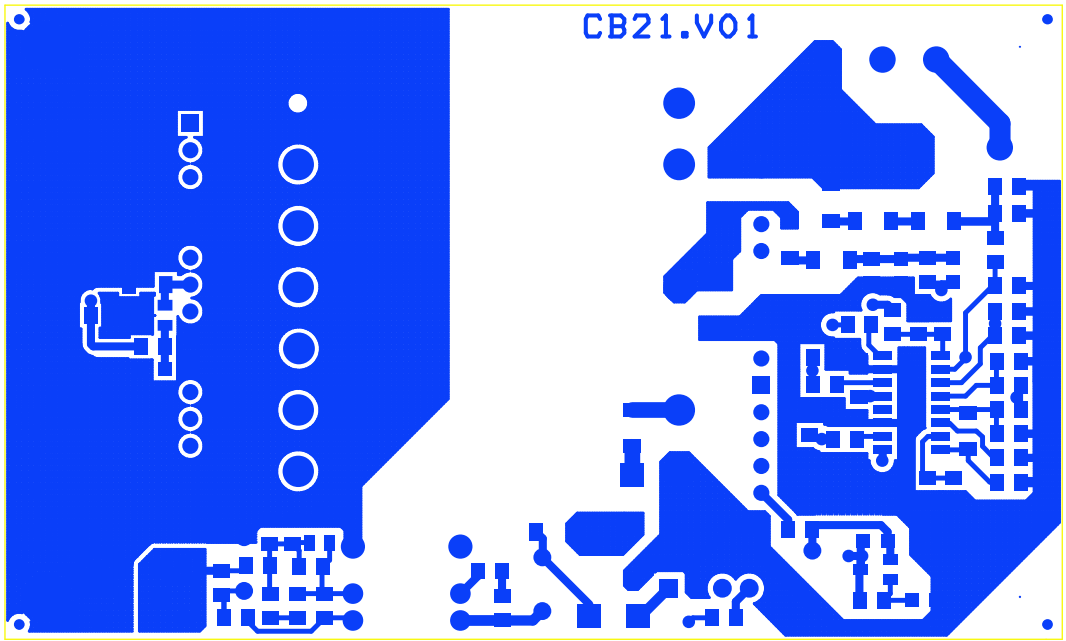


Figure 8. **EVLMG1-250WLLC motherboard PCB layout – top side**

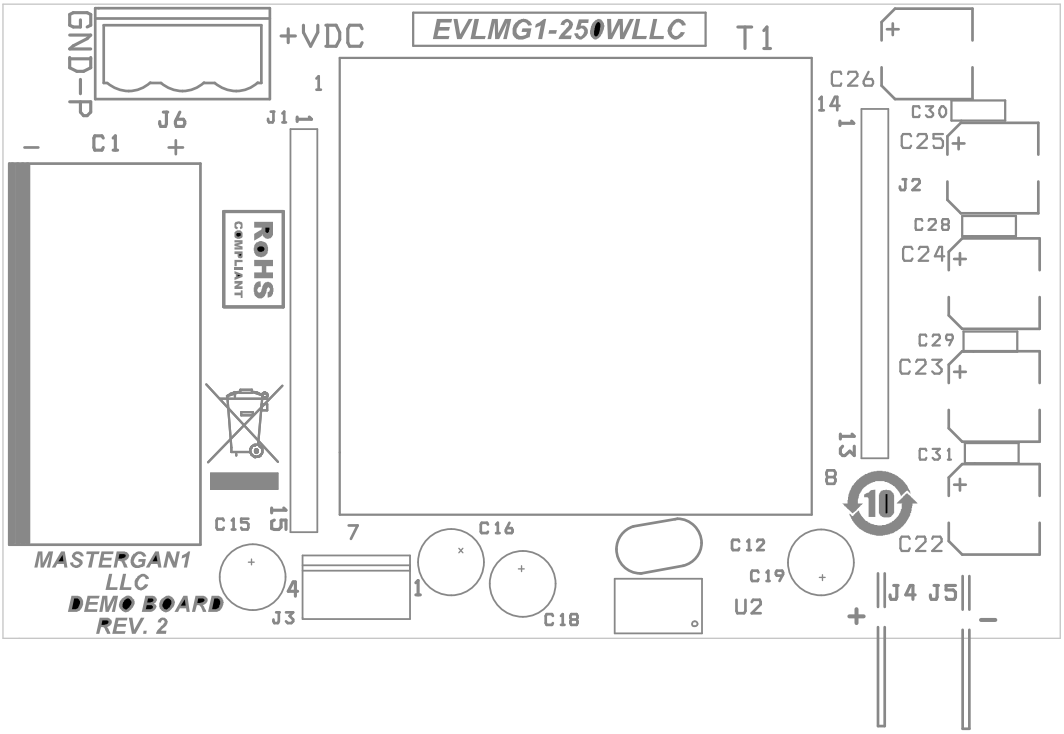


Figure 9. **EVLMG1-250WLLC motherboard PCB layout – bottom side**

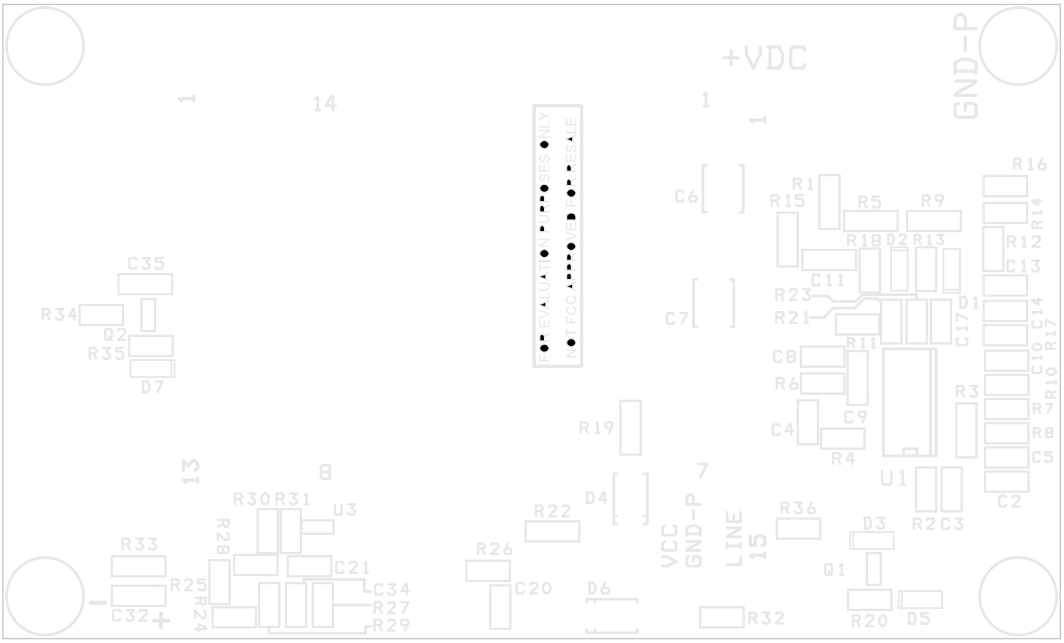


Figure 10. MasterGaN1 daughterboard PCB track – top side

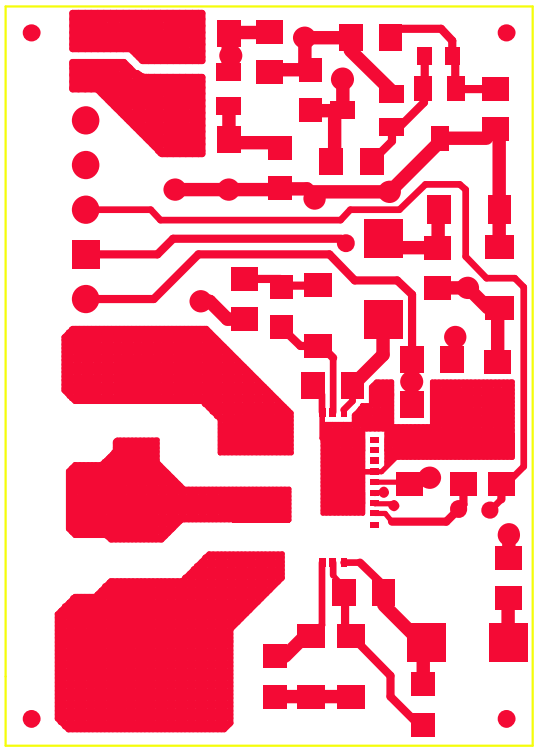


Figure 11. MasterGaN1 daughterboard PCB track – bottom side

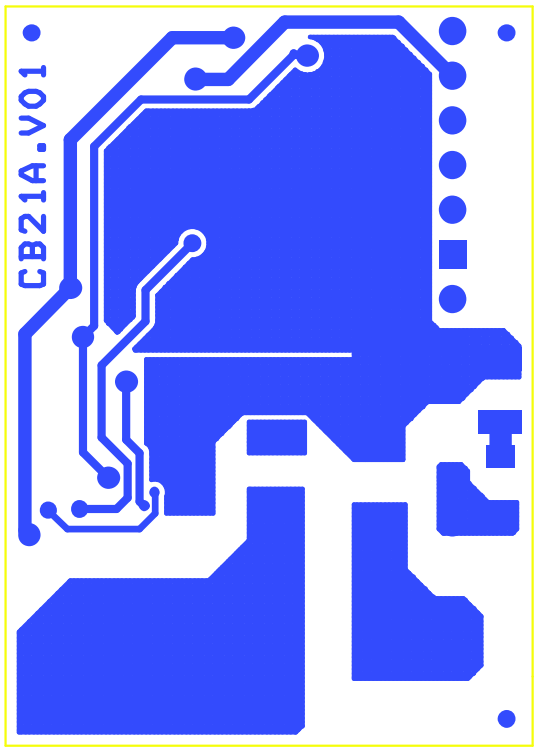


Figure 12. MasterGaN1 daughterboard PCB layout – top side

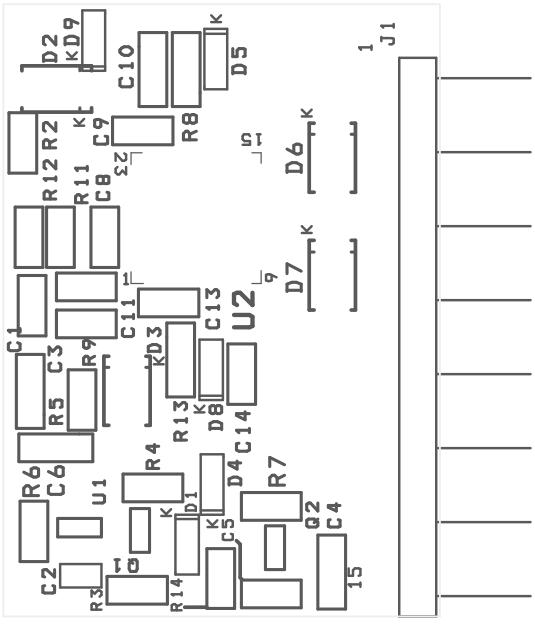


Figure 13. MasterGaN1 daughterboard PCB layout – bottom side

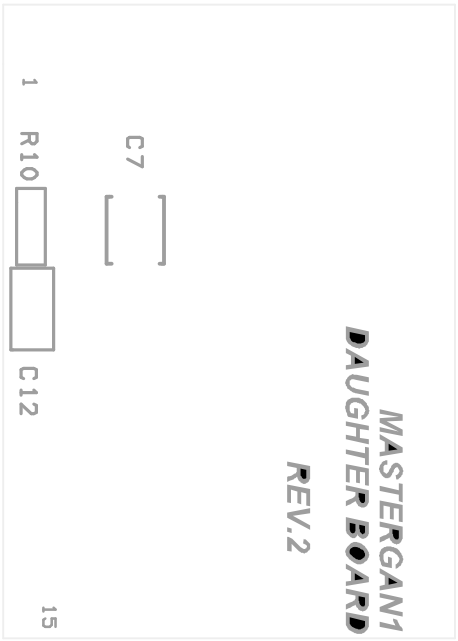


Figure 14. Synchronous rectifier daughterboard PCB tracks – top side

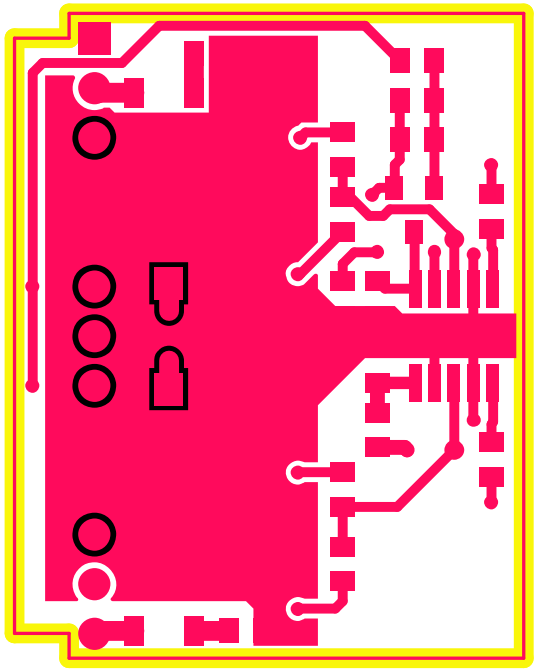


Figure 15. Synchronous rectifier daughterboard PCB tracks – bottom side

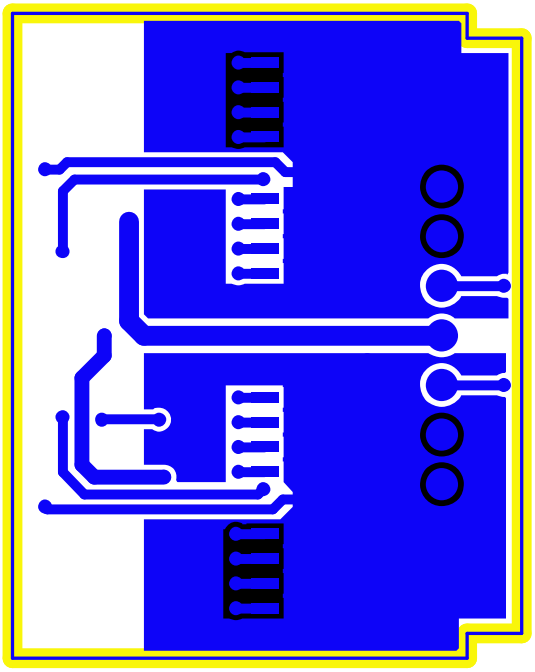


Figure 16. Synchronous rectifier daughterboard PCB layout – top side

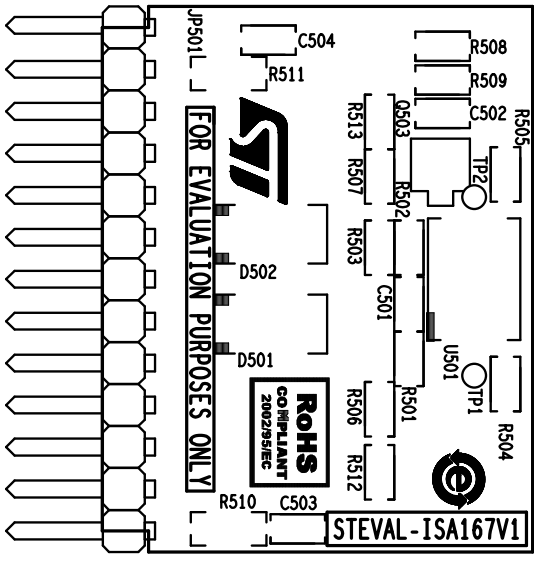
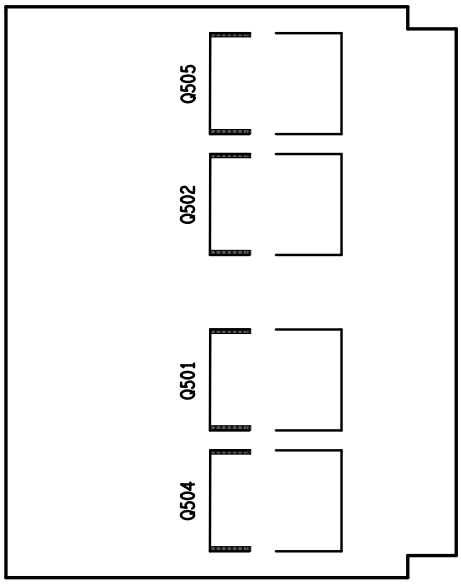


Figure 17. Synchronous rectifier daughterboard PCB layout – bottom side



3 EVLMG1-250WLLC description

The EVLMG1-250WLLC evaluation board is composed of one motherboard and two daughterboards (for MasterGaN1 and Secondary Synchronous rectifier) plugged on it. The EVLMG1-250WLLC is supplied by 400 Vdc (J6) as power rail; an additional 15 V referred to primary GND has to be provided to supply the control part on connector J3. This auxiliary voltage is needed just for startup, after startup the external auxiliary can be removed since the Vcc is self supplied via the primary transformer. The board is based on a resonant LLC topology, the working frequency at full load is around 260 KHz, output power is 250 W at 24 Vdc.

The power transformer is driven by the MasterGaN1, an advanced power system-in-package integrating a gate driver and two enhancement mode GaN FET connected in half-bridge configurations needed by the selected topology. MasterGaN1 is supplied by a linear regulator delivering 6.9 V, composed by Q1, U1, R3 and R6. This regulator voltage is used to supply the MasterGaN1 Vcc pin and via the diodes D2 and D3 the drivers of the low-side and the high-side FET. The control IC is the L6599A, a double ended controller dedicated to resonant half-bridge topology. It provides two output signals with 50% complementary duty cycle, 180º out-of-phase with a fixed deadtime inserted between the turn-off of one switch and the turn-on of the other one allowing the ZVS operation.

The L6599A allows to set the minimium and maximum operating frequency by R3, R7, R8 and C2, pin STBY allows to set the Burst mode threshold. In order to have the LLC stage activation with proper input voltage, the L6599A by means of a driver R1, R5, R9, R14, R16 connected to LINE pin, monitors the converter input voltage preventing operation with too low input voltage. Additional protections are OCP and output voltage loop fail, managed by pins ISEN and DIS.

To achieve high efficiency the board uses synchronous rectification on the secondary side, managed by SRK2001 driving the MOSFETs Q501 and Q502. This portion is located on the daughterboard located on the secondary side. A linear voltage regulator on the motherboard bottom side scales down o/p voltage supplyng the SRK2001.

4 EVLMG1-250WLLC board overview

Table 1 and Table 2 below list the EVLMG1-250WLLC characteristics and connectors.

Table 1. EVLMG1-250WLLC characteristics

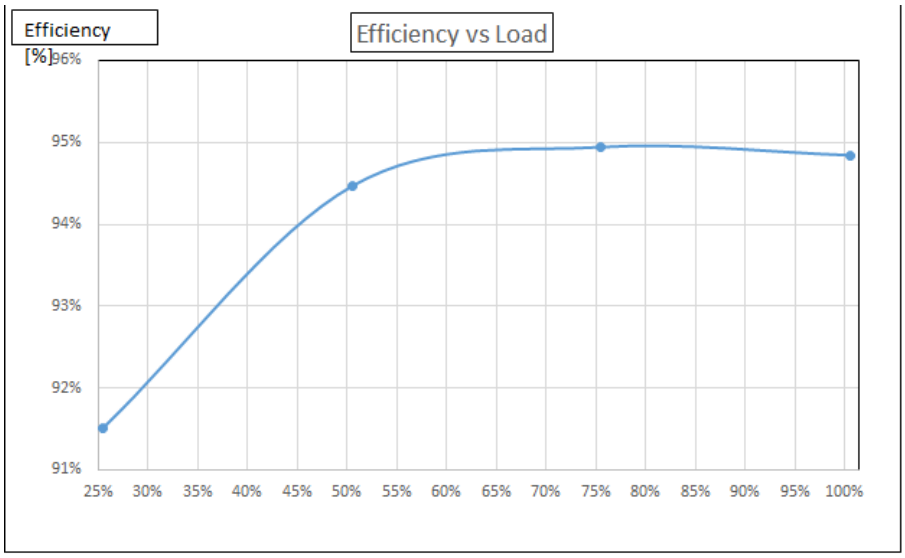
Parameter	Value
DC input voltage	400 V ±10%
DC output voltage	24 V
Output current	up to 10.4 A
Output power	Pout = 250 W
Efficiency	Eff. > 94% at full load
No load consumption	≤ 500 mW
Operating frequency @ full load 400 Vin	260±10 KHz
Output voltage loop fail protection	
Overcurrent/short-circuit protection	
Board size	100 x 60 (WxH) mm Maximum component height: 35 mm

Table 2. EVLMG1-250WLLC connectors

Reference	Type	Description
J1	Female-STRIP-15PINS	MasterGaN board
J2	Female-STRIP-13PINS	SR board
J3	PCB headers	Auxiliary input voltage
J4	Faston terminal (+)	Power output
J5	Faston terminal (-)	Power output
J6	PCB terminal	Power input

5 EVLMG1-250WLLC performance and efficiency measurement

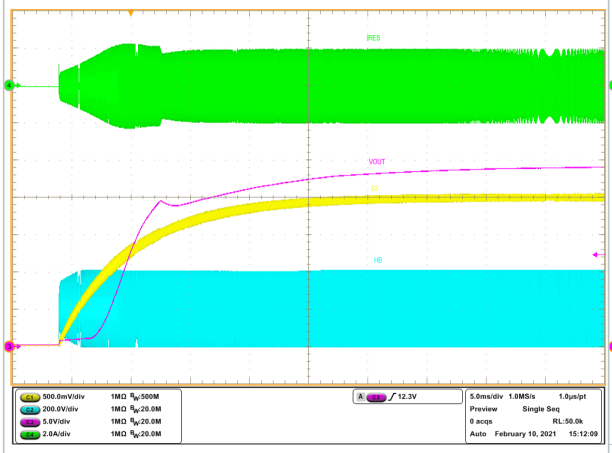
Figure 18. **EVLMG1-250WLLC efficiency**



In the above diagram the Efficiency measured from a 25% to 100% load is reported. At maximum output power the measured efficiency is over 94%.

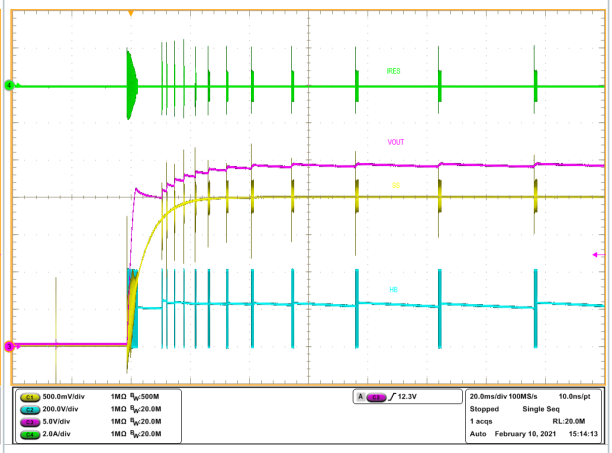
6 EVLMG1-250WLLC waveforms

Figure 19. Startup @ full load



Ch.1: Soft start pin; Ch.2: Half bridge; Ch.3: VOUT;
Ch.4: Resonant current

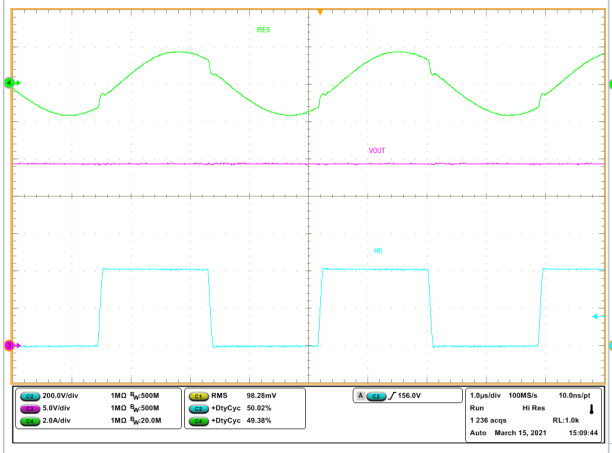
Figure 20. Startup @ no load



Ch.1: Soft start pin; Ch.2: Half bridge; Ch.3: VOUT;
Ch.4: Resonant current

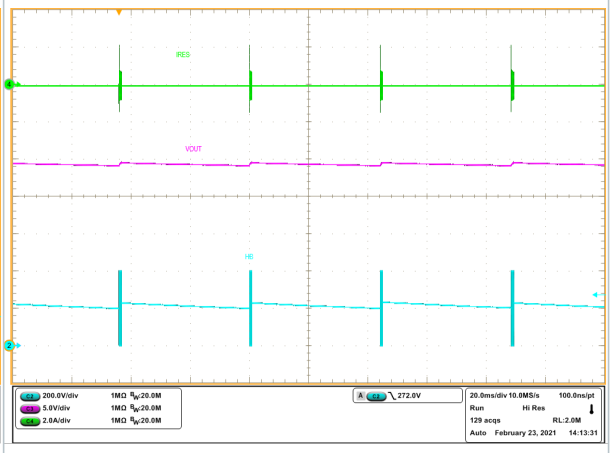
Figure 19 and Figure 20 show the startup operation in both full load and no load conditions.

Figure 21. Steady-state 8A load



Ch.2: Half bridge; Ch.3: VOUT; Ch.4: Resonant current

Figure 22. Steady-state @ no load

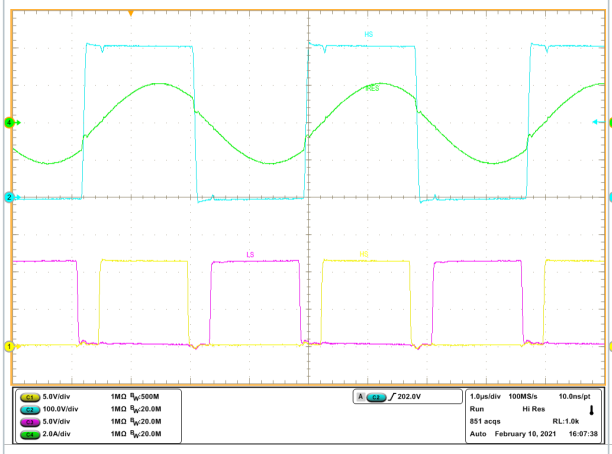


Ch.2: Half Bridge; Ch.3: VOUT; Ch.4: Resonant current

Figure 21 and Figure 22 show the steady-state operations at 8A and no load conditions (burst mode).

Figure 23 and Figure 24 show the steady-state conditions at full and half load: HVG and LVG signals from the L6599A are shown as reference.

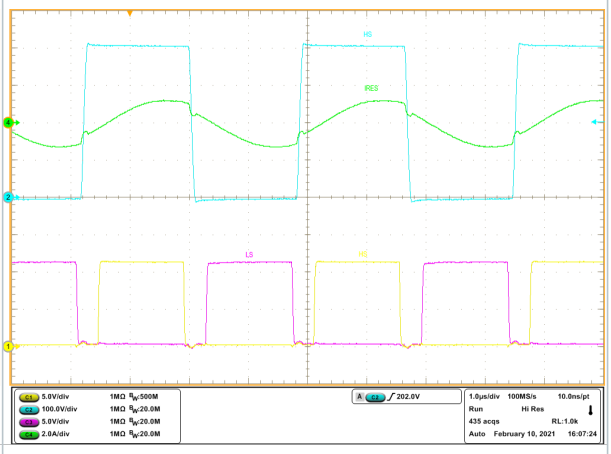
Figure 23. Switching activity steady-state FL



Ch.1: HVG; Ch.2: Half bridge voltage; Ch.3: LVG;

Ch.4: Resonant tank current

Figure 24. Switching activity steady-state HL

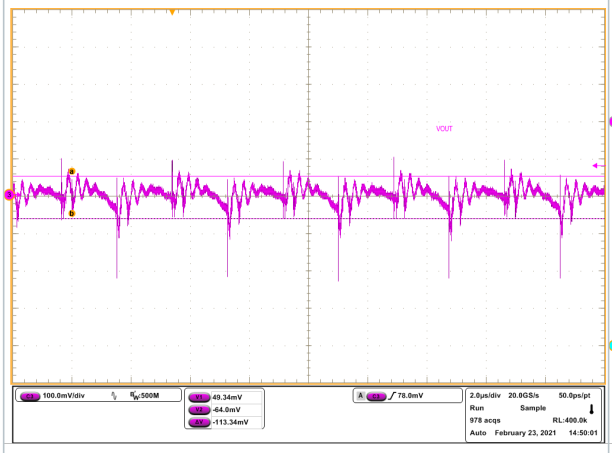


Ch.1: HVG; Ch.2: Half bridge voltage; Ch.3: LVG;

Ch.4: Resonant tank current

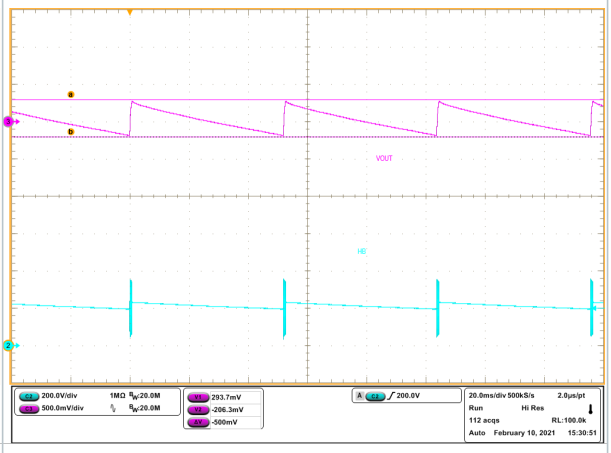
Figure 25 and Figure 26 show the output voltage ripple. The Vpeak to peak ripple are 120 mV at full load and 500 mV at no load during burst mode operation.

Figure 25. Vout ripple full load



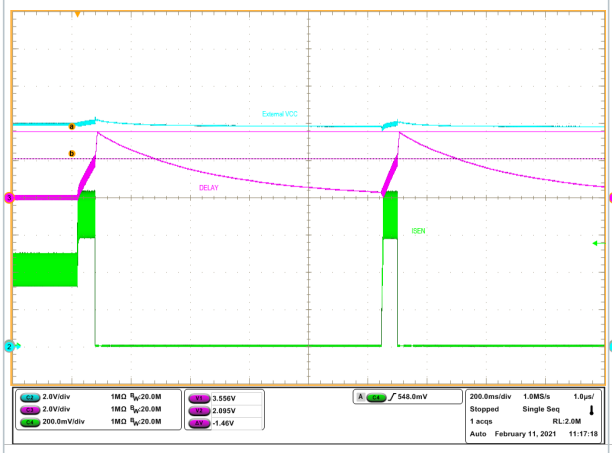
Ch.3: VOUT ripple

Figure 26. Vout ripple no load



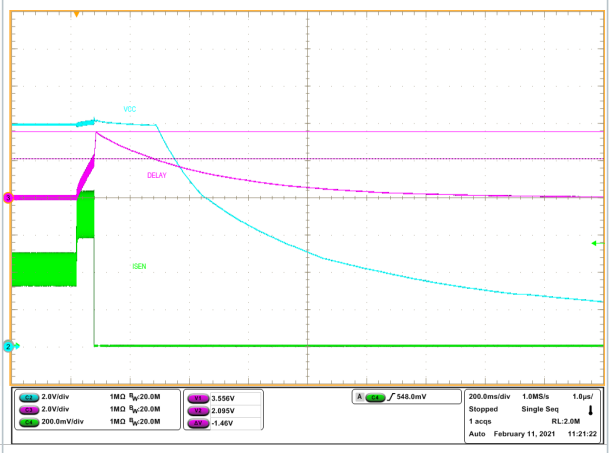
Ch.2: Half bridge; Ch.3: VOUT ripple

Figure 27. Overcurrent protection with ext. VCC



Ch.2: external VCC; Ch.3: Delay pin; Ch.4: ISEN pin

Figure 28. Overcurrent protection without ext. VCC

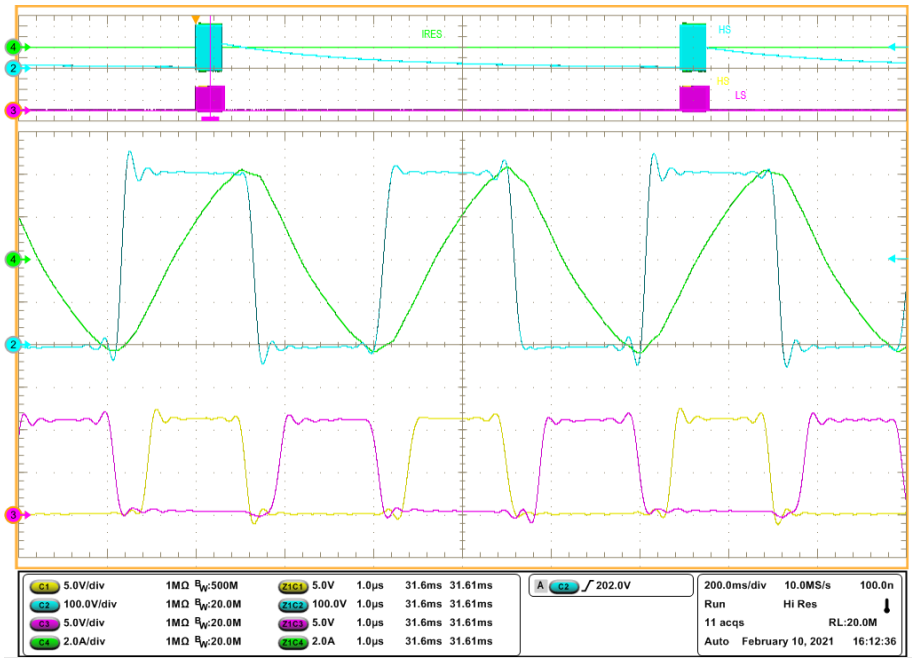


Ch.2: VCC; Ch.3: Delay pin; Ch.4: ISEN pin

The EVLMG1-250WLLC evaluation board is protected by short-circuit or overcurrent which might occur, preventing component overheating or catastrophic failures of the board. Figure 27 and Figure 28 show the safe interruption of switching activity. In Figure 27, since the board is supplied by an external Vcc, it can be observed that the board starts working in hiccup mode until the short is removed. Then it restarts via a soft-start cycle. In Figure 28, since the external Vcc is removed and the board is self supplied, we can see that after the short is applied the converter works for a short time then it stops the operation because the Vcc is lost and the converter cannot restart. To resume operation it is necessary to reconnect the external Vcc allowing the board startup.

Figure 29 shows the significant waveforms of hiccup mode in short-circuit condition.

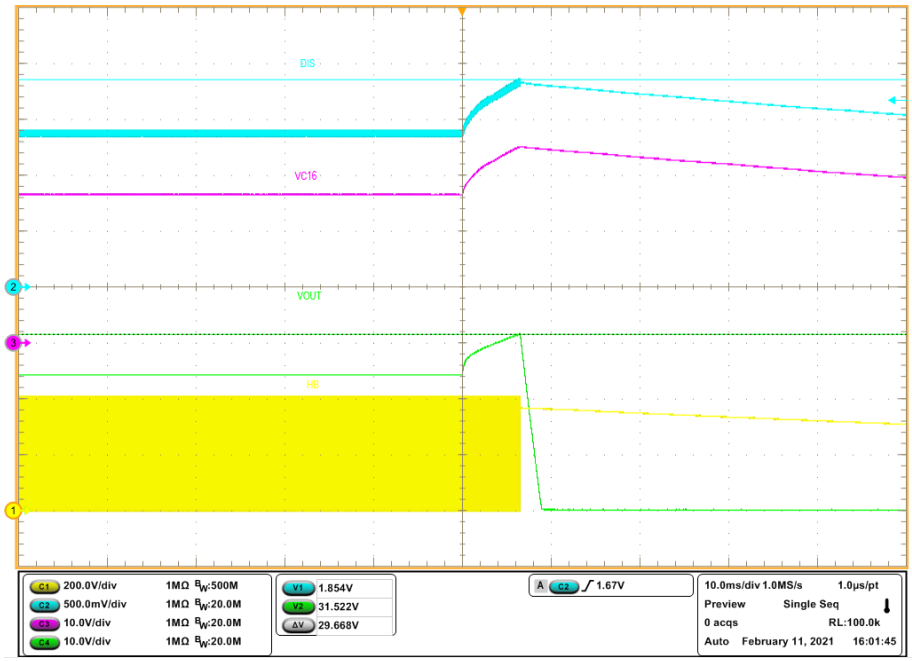
Figure 29. OCP switching activity detail



Ch.1: HVG; Ch.2: Half bridge; Ch.3: LVG; Ch.4: Resonant current

An additional protection of the EVLMG1-250WLLC evaluation board is the open loop failures protection, sensing the auxiliary voltage. As shown in Figure 29, in case of output voltage loop fail, the auxiliary voltage Vaux rises and once the voltage on the DIS pin has reached the 1.85 V threshold, the L6599A stops operation and latches the switching activity. The converter operation is resumed after the Vcc has dropped below the UVLO threshold. The measured Vout is 31.5 V, below the maximum voltage rating of the output capacitors.

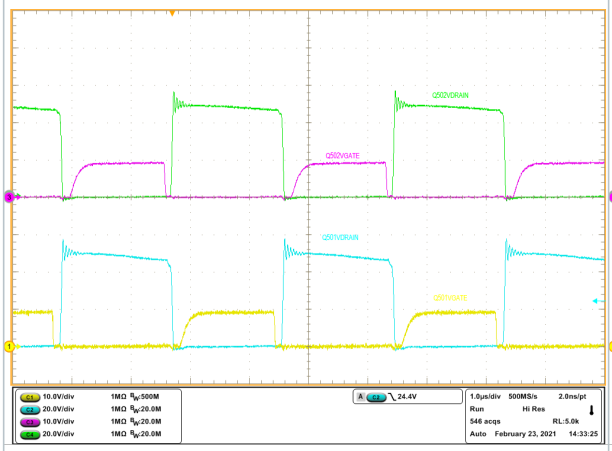
Figure 30. Overvoltage protection



Ch.1: Half bridge; Ch.2: L6599A DIS pin; Ch.3: VC16; Ch.4: VOUT

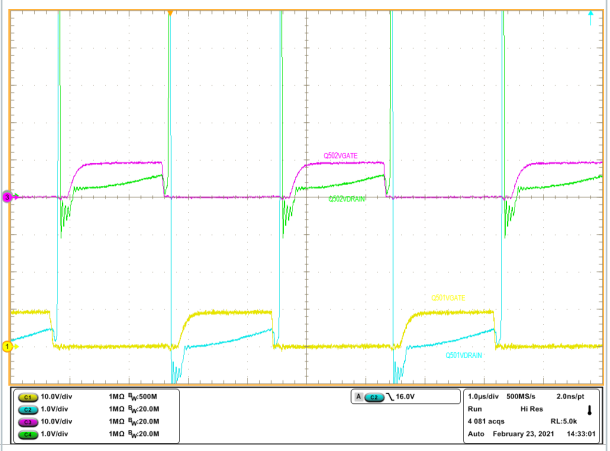
Figure 31 shows the drain and gate voltages of secondary MOSFETs driven by the SRK2001, synchronous rectifier controller. Figure 32 shows the detail of the secondary MOSFET's drain voltage. The voltage drop variation before and after each MOSFET turn-on and turn-off.

Figure 31. SR waveforms



Ch.1: Q501 gate voltage; Ch.2: Q501 drain voltage;
Ch.3: Q502 gate voltage; Ch.4: Q502 drain voltage

Figure 32. SR drain voltage detail



Ch.1: Q501 gate voltage; Ch.2: Q501 drain voltage;
Ch.3: Q502 gate voltage; Ch.4: Q502 drain voltage

In Figure 33 the EVLMG1-250WLLC evaluation board thermal map at full load is reported.

Figure 33. Thermal map full load (250 W)

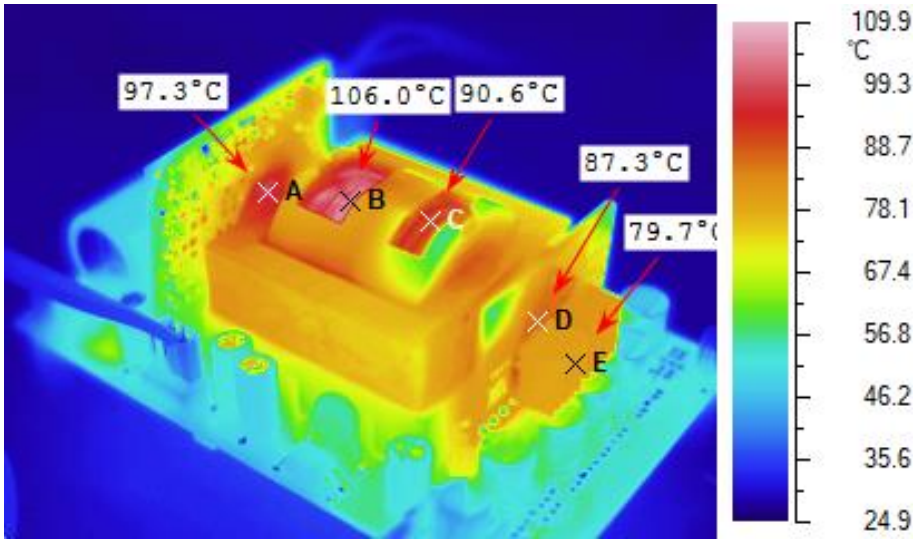


Table 3. Thermal map, points description

A: MasteraGaN1	D: Secondary Mosfet
B: Primary Trafo	E: Heat Sink Secondary Mosfet
C: Secondary Trafo	

7 References

MasterGaN1 Datasheet: DS13417 (see www.st.com)
L6599A Datasheet: DS6027 (see www.st.com)
SRK2001 Datasheet: DS10811 (see www.st.com)

Revision history

Table 4. **Document revision history**

Date	Version	Changes
12-Apr-2021	1	Initial release.

Contents

List of tables

List of figures